b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

6. (Amended) The memory system according to claim 5, wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of one of the plurality of pipelined memory subsystems and a second delay introduced by the data register of one of the plurality of pipelined memory subsystems.

29. (Amended) A method [for] of retrieving data in a pipelined memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising [the steps of]:

issuing commands and addresses on a unidirectional command and address bus;

latching the commands and addresses in the [a plurality of] buffer registers;

driving the latched commands and addresses to the column and row decoders [a plurality of memory devices having addressable storage];

retrieving [the] data from the addressable storage of one of the plurality of memory devices;

latching the data in [a] the data registers; and

receiving the data on a bidirectional data bus.

30. (Amended) The [memory system] method of retrieving data according to claim 29 wherein each of the memory devices is a dynamic random access memory device.

31. (Amended) The method of [storing information] retrieving data in a pipelined memory system according to claim 29 wherein [the step of communicating] issuing commands and addresses and [the step of communicating] receiving data communicates according to a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

32. (New) A method of storing data in a pipelined memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses in the plurality of buffer registers;

latching the data in the plurality of data registers;

driving the latched commands and addresses to the column and row decoders;

driving the latched data to the data in buffers; and

storing the data in the addressable storage of the plurality of memory devices.

33. (New) The method of claim 32, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the buffer register of one of the plurality of memory subsystems and a second delay introduced by the data register of one of the plurality of memory subsystems.

34. (New) An electronic system comprising:

a microprocessor;

a memory controller coupled to the microprocessor;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a) a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

35. (New) The electronic system of claim 34, wherein the memory controller communicates the commands and addresses and data information using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of one of the plurality of pipelined memory subsystems and a second delay introduced by the data register of one of the plurality of pipelined memory subsystems.

36. (New) The electronic system of claim 34, wherein each memory device is a dynamic random access memory device.

37. (New) The electronic system of claim 34, wherein both M and N equal eight.

38. (New) A method of performing a memory transaction in an electronic system having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing information to the memory controller;

issuing commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses received from the unidirectional command and address bus in the buffer registers of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices; and

if the memory transaction is a write, receiving and latching the data in the data registers of the plurality of memory subsystems and driving the latched data to the plurality of memory devices.

39. (New) The method of claim 38, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

40. (New) A method of storing data, in an electronic system, having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses read from the unidirectional command and address bus in the buffer registers of the plurality of memory subsystems;

latching the data received from the bidirectional data bus in the data registers of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices;

driving the latched data to the plurality of memory devices; and

storing the data in addressable storage of the plurality of memory devices.

41. (New) The method of claim 40, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

42. (New) In an electronic system having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, a method of retrieving data comprising:

issuing information to the memory controller;

issuing commands and addresses on a unidirectional command and address bus;

latching the commands and addresses read from the unidirectional command and address bus in the buffer registers of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices of the plurality of memory subsystems;

retrieving data from addressable storage of the plurality of memory devices of the plurality of memory subsystems;

latching the data in the data register of the plurality of memory devices of the plurality of memory subsystems; and

receiving the data on a bidirectional data bus.

43. (New) The method of claim 42, wherein issuing commands and addresses and receiving data include executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

44. (New) A memory system comprising:

a unidirectional command and address bus coupleable to a memory control device;

a bidirectional data bus coupleable to the memory control device; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a) a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

45. (New) The memory system of claim 44, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of one of the plurality of pipelined memory subsystems and a

second delay introduced by the data register of one of the plurality of pipelined memory subsystems.

46. (New) The memory system of claim 44, wherein each memory device is a dynamic random access memory device.

47. (New) The memory system of claim 44, wherein both M and N equal eight.

48. (New) A method of storing data in a pipeline memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

receiving commands and addresses from a unidirectional command and address bus;

receiving data from a bidirectional data bus;

latching the commands and addresses in the plurality of buffer registers;

latching the data in the plurality of data registers;

driving the latched commands and addresses to the column and row decoders;

driving the latched data to the data in buffers; and

storing the data in the addressable storage of the plurality of memory devices.

49. (New) The method of claim 48, wherein receiving commands and addresses and receiving data include executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

50. (New) A method of retrieving data in a pipeline memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a buffer register, a data register and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

receiving commands and addresses from a unidirectional command and address bus;
latching the commands and addresses in the plurality of buffer registers;
driving the latched commands and addresses to the column and row decoders;
retrieving data from the addressable storage of the plurality of memory devices;
latching the data in the plurality of data registers; and
driving the data onto a data bus.

51. (New) The method of claim 50, wherein receiving commands and addresses and driving the data include executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

52. (New) A memory system, comprising:

a unidirectional command and address bus in electrical communication with a memory control device;

a bidirectional data bus in electrical communication with the memory control device; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a) a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from

the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

53. (New) The memory system of claim 52, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of one of the plurality of pipelined memory subsystems and a second delay introduced by the data register of one of the plurality of pipelined memory subsystems.

54. (New) The memory system of claim 52, wherein each memory device is a dynamic memory device.

55. (New) The memory system of claim 52, wherein both N and M equal eight.

56. (New) A method of retrieving data in a pipelined memory system, comprising:

issuing commands and addresses on a unidirectional command and address bus to a plurality of memory subsystems;

latching the commands and addresses in a buffer register in each of the plurality of memory subsystems;

driving the latched commands and addresses to column and row decoders in each of the plurality of subsystems;

retrieving data from addressable storage of one of the plurality of memory subsystems;

latching the data in a data register of the one of the plurality of memory subsystems; and

receiving the data on a bidirectional data bus.